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Software Design of Microprocessor-Controlled Receivers Part 2

WATKINS-JOHNSON COMPANY

Tech-notes

Part 1 of this article discussed mainly the AGC software portion of the receiver. Part 2 will discuss AFC, BFO and Fast Scan software.

AFC in Software

Automatic frequency control (AFC), in a conventional receiver, is used to follow a drifting signal or to correct for a local oscillator that is drifting with time and temperature. Conventional receivers provide feedback from the frequency discriminators back to a varactor in the local oscillator tank circuit to accomplish frequency stability. Synthesized local oscillators do not drift, and most transmitted signals are crystal controlled. AFC in a microprocessor-controlled receiver is most commonly used to center a signal in the IF passband when in the scan mode of operation. A frequency scan may stop on the edge of a signal that exceeds the COR THRESHOLD, but is not sufficiently centered within the receiver IF passband to be properly demodulated until the receiver is retuned. Software-controlled AFC uses the DC voltage output from the frequency discriminators, in digital form, to retune the receiver and center the signal within the IF passband. Several variations in AFC characteristics are possible by reprogramming the capture and holding range. In the block diagram in Figure 1, notice the similarity to the previous block diagrams.

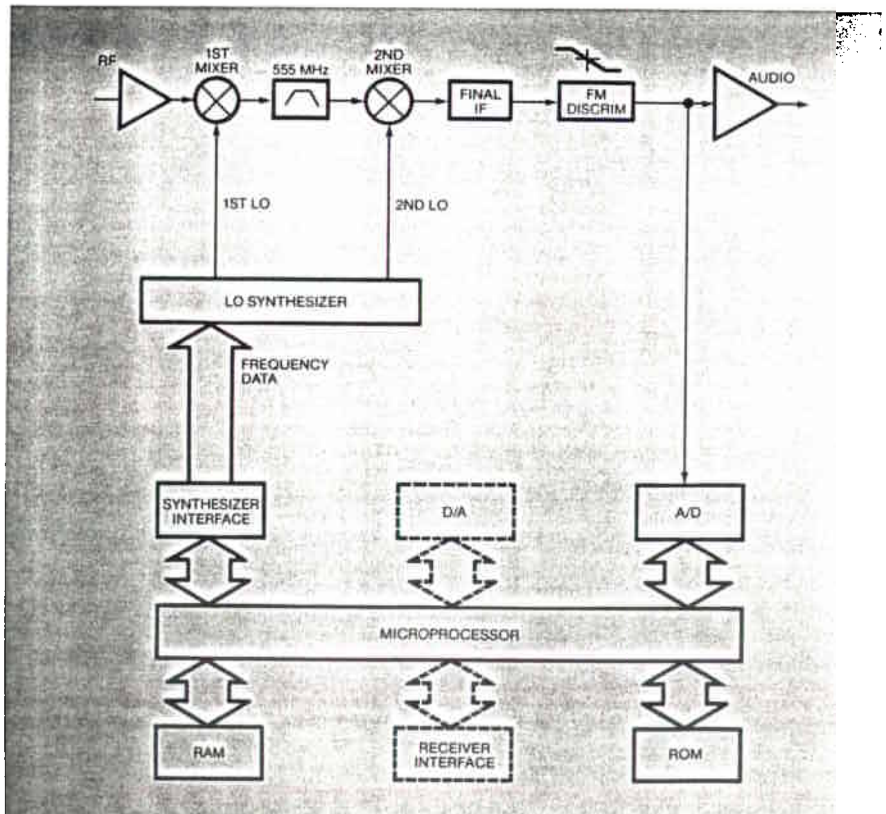

Figure 1. Software-controlled AFC.

Overview of Software AFC

In a software AFC system, the mirco-processor determines where the signal is by sampling the average DC level at the output of the FM discriminator. It then retunes the receiver to the signal frequency. In this system, any FM modulation must be stripped from the discriminator output so the receiver does not try to track with the modulation. This can be done with either software or hardware. The hardware approach is often selected to simplify the software. Software AFC has no design limits that prevent it from tracking a signal from one end of the tuning range to the other. However, to make its operation more conventional, a correction limit of 10 bandwidths is placed in the software. If the required correction exceeds this limit, the software returns the receiver to the original tuned frequency. If a tune command is issued to the receiver from the tuning wheel or the remote bus, AFC is disabled, and the receiver tunes to the new frequency. AFC is then re-enabled with the new frequency used to compute the correction limits. Software AFC is natural for a microprocessor-controlled receiver. It requires only an A/D conversion of the FM discriminator.

AFC Flow Chart

The following paragraphs will explain the AFC operation using the flow chart in Figure 2. The first check made is to verify that all LOs are locked before the FM discriminator is read, to prevent false information from being fed back to the software. Now the FM discriminator is read, and the reading is tested to determine if it is within 10% of the center frequency. The AM detector is also read to verify that the COR indicator is active. A correction is now made up to 100% of the selected bandwidth in multiples of 10% of that bandwidth. The number of corrections is then tested for the 10-bandwidth limit. A failure of that test causes the frequency to be reset. A pass allows exit of AFC CONTROL, as does a failure of any of the signal-present tests.

Variable BFO in Software

Variable BFO is used to provide a tone for CW reception and to clarify single-sideband reception. A product detector creates this tone from the CW signal and the BFO injections. Conventional variable BFO uses a 21.4 MHz crystal oscillator that can be pulled ±4 kHz with 10-Hz resolution. For accurate resettability, the oscillator is followed by a ÷ N counter and compared through a phase detector to a fixed reference signal. The microprocessor changes the ÷ N number to agree with the offset frequency desired.

A fully synthesized variable BFO uses several times the circuitry that a simple variable oscillator needs. However, software design can program the desired offset frequency and stability with most of the circuitry of Figure 3 not needed. The oscillator frequency is divided by 2 and compared to an existing 10.7 MHz frequency. The phase comparator provides a difference frequency from either the higher or lower port. The microprocessor's software commands the difference frequency to be counted and compared to the desired offset on the front panel or remote bus. A calculated voltage is sent back to the variable crystal oscillator, which is continually corrected until the offset is reached. A block diagram shown in Figure 4 compares the circuitry to conventional BFO.

Overview of Software-Controlled BFO

The software-controlled BFO uses a microprocessor to close the loop bet-

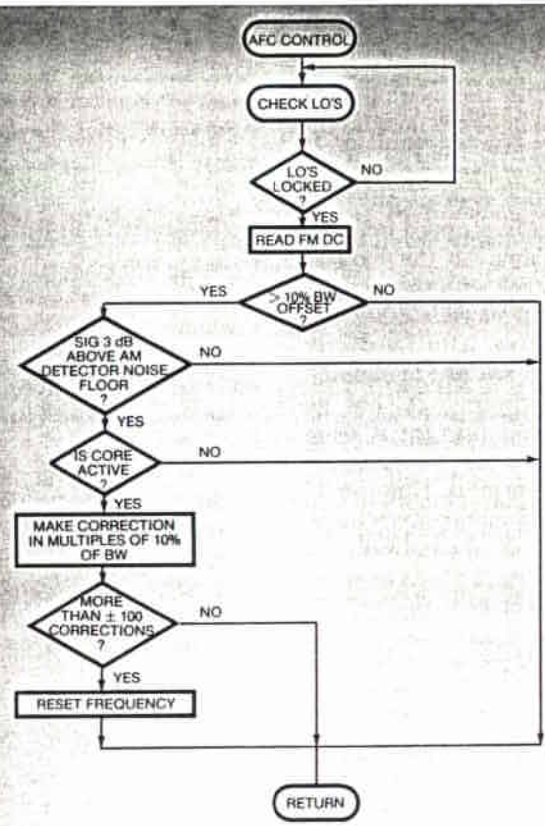

Figure 2. Flow chart of software AFC control.

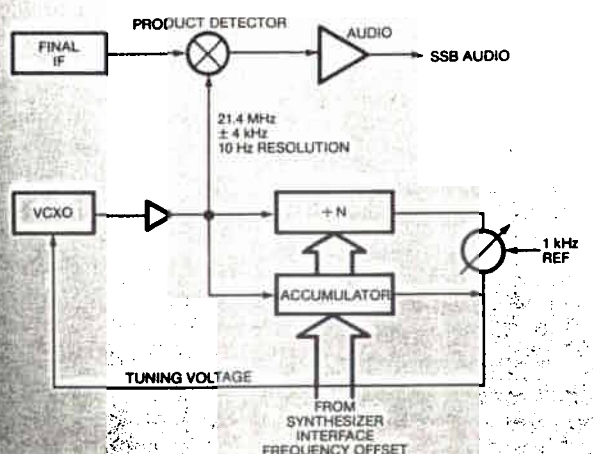

Figure 3. Conventional variable BFO.

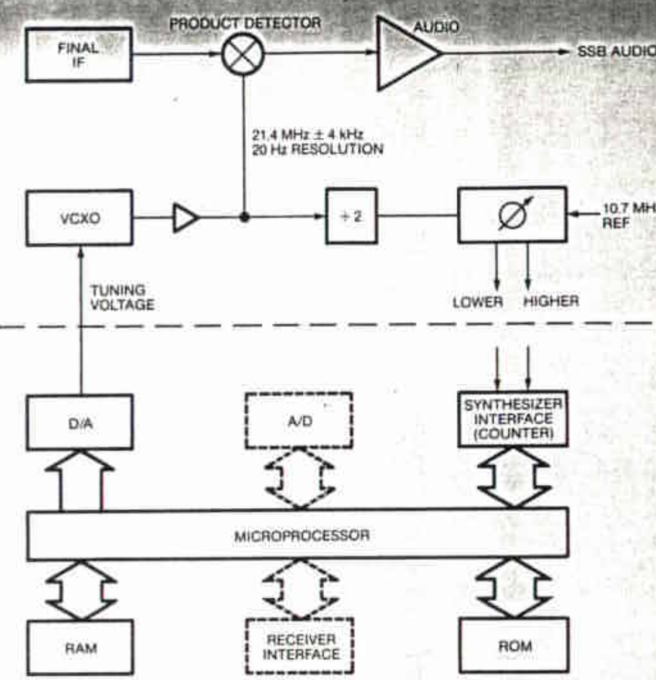

Figure 4. Software-controlled variable BFO.

ween the BFO oscillator and a frequency counter. This creates a software frequency-locked oscillator. A frequency counter measures the offset frequency of the BFO, then makes a decision on whether to make a correction from 40 to 400 Hz. If the needed correction is greater than 1 kHz, the software shifts to major correction where it calculates the required voltage to get the correct frequency and sends it. The correction is then returned to servo mode.

BFO Flow Chart

The BFO flow chart is shown in Figure 5. When the BFO FREQUENCY COUNTER is read, if the counter is within 1 count of the display, no correction is made. The counter is restarted and BFO CONTROL is exited. In the event the counter is off more than 25 counts (1 kHz in CW, 500 Hz in SSB), the voltage for the oscillator is calculated. If error is less than 25 counts, a correction is made to a maximum of 10 counts (400 Hz in CW, 200 Hz in SSB), then the counter is restarted and BFO is exited. (The counter sampling process takes 50 ms, so settling to a new frequency is typically less than 0.5 seconds.)

Fast Scan and Steps in Software

There is a great need for fast-scanning and stepping receivers in today's world of push-to-talk and frequency-hopping signals. The key to agile frequency receiver design is both fast synthesizer tuning speed and microprocessor speed, with no compromise in spectral purity. Digital agility in the past has always exceeded the indirect synthesizer tuning speed. The lockup time for a synthesizer is directly related to the

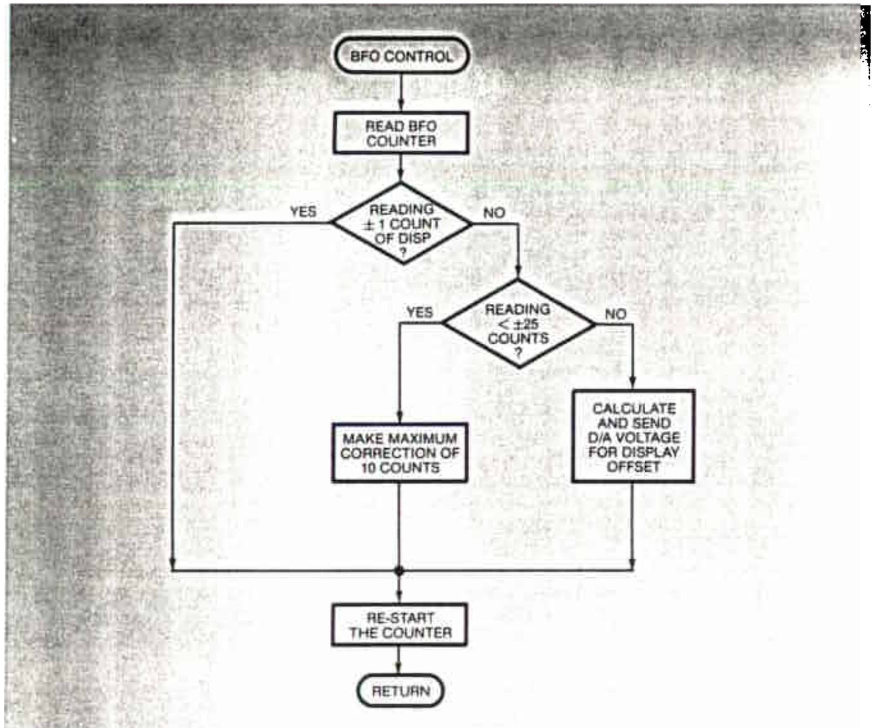

Figure 5. Flow chart of software BFO control.

reciprocal of the loop bandwidth, which is related to the tuning resolution and reference frequency. On the other hand, non-synthesized analog scans, can be done a hundred times faster, but are inherently poor in frequency accuracy and stability.

LO Synthesizers

The 1st LO synthesizer shown in Figure 6 was borrowed from the WJ-8618B. A transmission-line oscillator is used, operating on the 5th, 7th and 9th overtones. Overtone operation gives the oscillator excellent spectral purity. The pin diode selectively shunts out the end of the transmission line, changing the electrical length. The combination of line-length changes and overtones multiply to give the oscillator well over 30 discrete frequency bands.

A software routine controls the pin diodes to select which band works best at each frequency for the lowest possible phase noise. The pin diode combination resides on the synthesizer in EPROM form. To reduce the module size, this low phase noise oscillator was changed for the WJ-8615D to tune from 557 MHz to 1075 MHz in 5-MHz steps. The reference frequency is 2.5 MHz, and inherently allows a frequency switching speed of 300 microseconds.

The 2nd LO synthesizer is shown in Figure 7. The long divide by N and low reference frequency of 10 kHz predict a long lockup time, on the order of 50 milliseconds. The 2nd LO VCO has a special tank circuit similar to the 1st LO synthesizer. A transmission line semi-rigid cable is cut in length to be a quarter wave length at 1/5th the oscil-

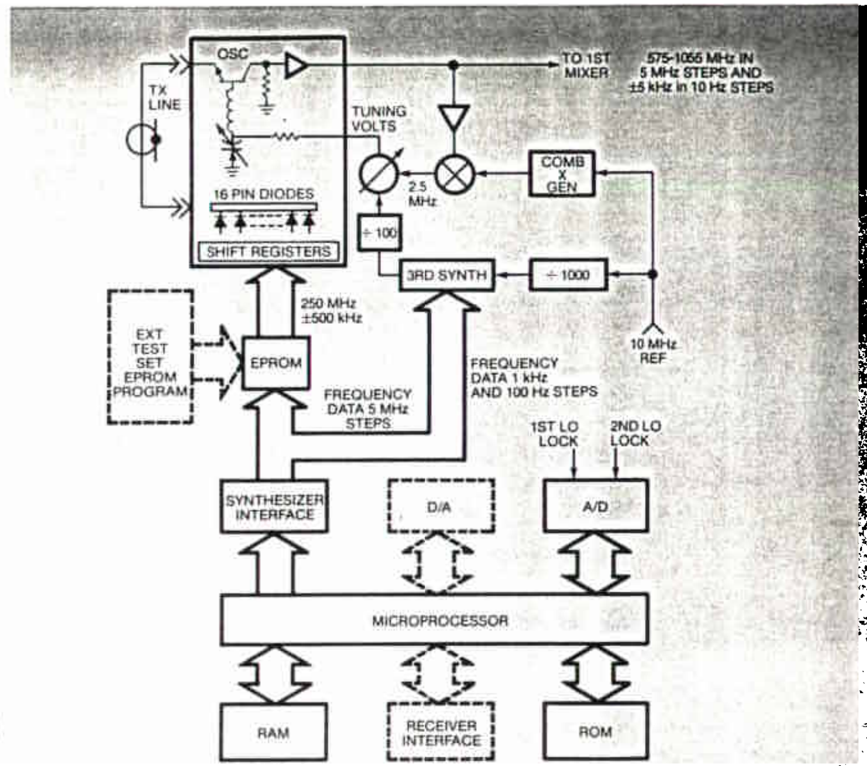

Figure 6. 1st LO synthesizer.

lator frequency of 530-535 MHz. A varactor-controlled tank circuit resonates the transistor base at the wanted frequency while the emitter looks at the 5th overtone of the transmission line. This oscillator is very low noise and exceptionally stable over temperature, shock and vibration, and time. Frequency drifts of no greater than 200 kHz from 0 to 50°C can be expected.

Overview of Fast Scan

The stability of the LO frequency is the key to a unique fast-scan routine that duplicates the speed of an analog scan with the accuracy of a synthesizer. When commanded to do a calibration, the microprocessor sends a coarse tuning voltage to the oscillator, waits for lockup, and then measures the voltage needed for the fine-tune varactor at this frequency. The voltage value on the coarse tuning varactor is adjusted until the fine-tune voltage is at an exact value. The revised voltage value is stored in RAM for that value, and all values needed every 10 kHz, over the 5-MHz LO range. This calibration process takes about 90 seconds. The microprocessor can now command a scan or step to within 3 kHz of any frequency. Periodically, before a scan, a small amount of time is used to calibrate a frequency point to compensate for long-term drift. Scan times per step can be expected to take less than 400 microseconds. A scanning speed of 400 microseconds per step is commensurate with

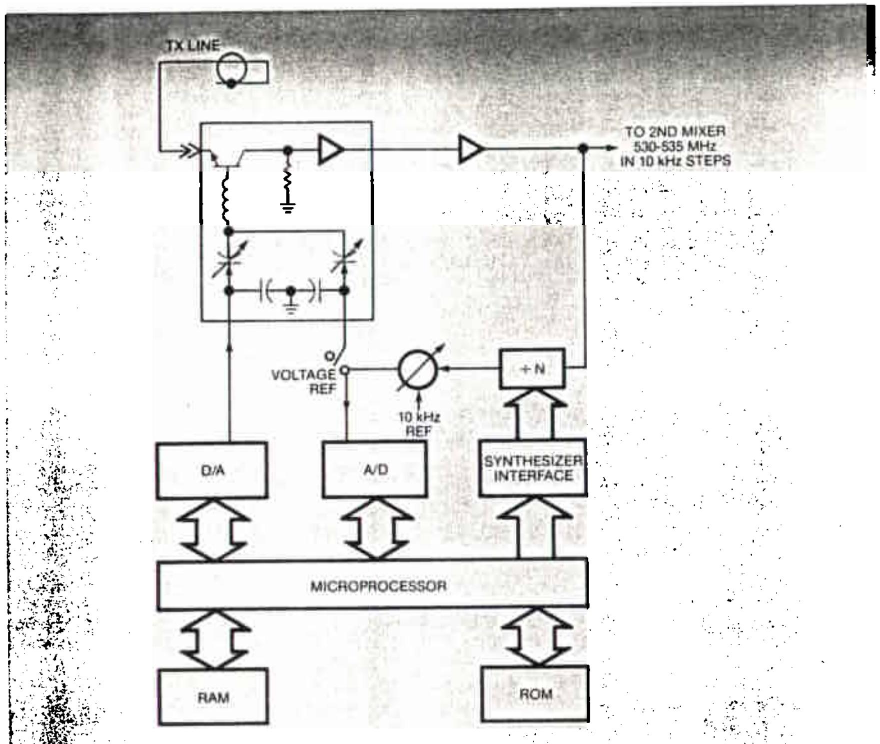

Figure 7. 2nd LO synthesizer with software fast-scan learn mode.

a 15-25 kHz IF bandwidth and, therefore, is compatible with most frequency-hopping and push-to-talk transmissions.

Discussion of Fast Scan Flow Charts

FAST SCAN flow charts appear in Figures 8 and 9. They show the operation of the fast-scan and scan-calibration logic. The first operation is to do the calibration scan.

The CALIBRATION SCAN tunes the 2nd LO across those frequencies that will be used in the scan, and creates a voltage code for each required frequency. Using a 12-bit A/D, which generates 4096 possible voltages, it is possible to step the second LO in 5-kHz increments by interpolating the voltage between 2 locked points, 10 kHz apart. The calibration routine first calculates the first frequency in the scan to which the 2nd LO will be tuned and the number of points in the total scan. During the entire calibration process the frequency display will show "CAL SCN." Now the 2nd LO is tuned to the first scan frequency and the software waits for the LO lock indication. The fine tuning voltage to the 2nd LO is read and compared to the reference voltage that will be used when the LO is open looped. The coarse tune will be adjusted until the fine tune voltage equals the reference. This code, or the interpolated code, will be stored in a SCAN RAM location. Now the frequency word is tested for the last 2nd LO frequency of the scan; if it is the last point, a flag is set in the SCAN RAM

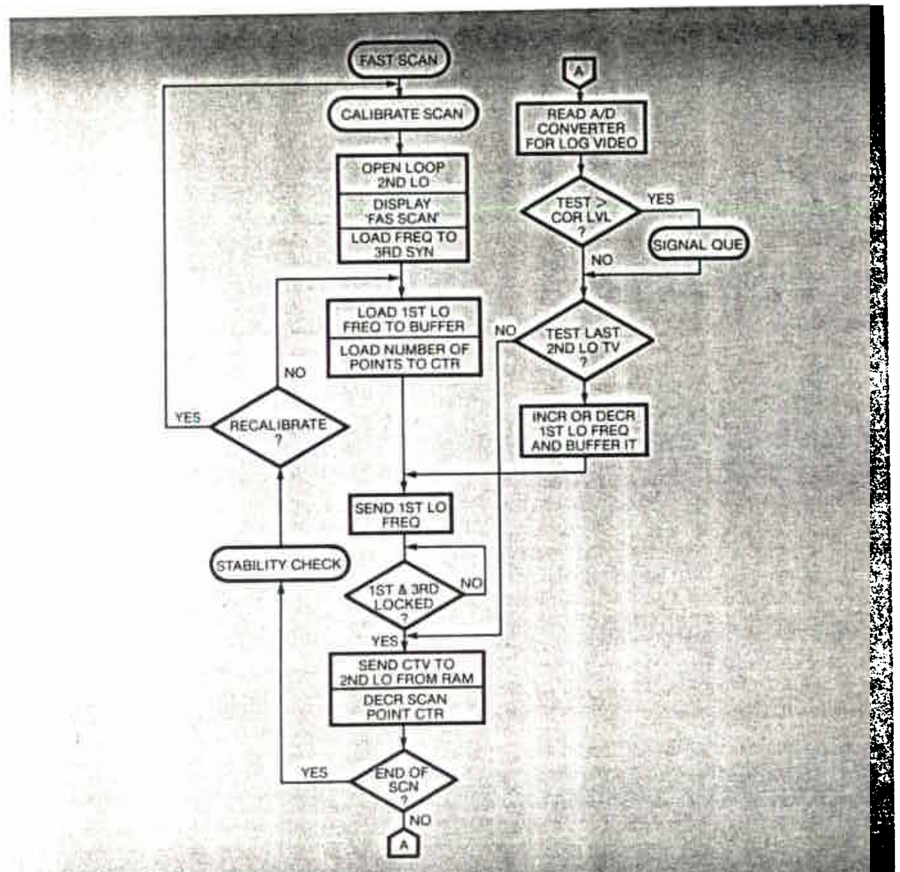

Figure 8. Flow chart of fast-scan operation.

tuning word and the calibration is complete. Otherwise, the new 2nd LO frequency is calculated and loaded, and the tuning loop is repeated. This completes the calibration.

The actual scan will consist of loading the voltage codes from the SCAN RAM to the D/A. Then, at 1st LO change points, the SCAN RAM table is started over. After the calibration, the 2nd LO is open-looped with the fine-tuning voltage connected to the reference, the 3rd LO frequency loaded and "FAS SCN" displayed in the frequency window. This completes the setup for the scan.

Inside the major loop, the 1st LO frequency is transferred to a buffer along with the number of scan points being transferred to the SCAN POINT COUNTER. The 3rd and 1st LO lock indicators are checked.

Now we enter the actual FAST SCAN loop. The voltage code found during the calibration is loaded to the 2nd LO coarse tune D/A. The scan point counter is decremented and tested for end-of-scan. If end-of-scan is detected, a stability check is done on the 2nd LO. When found in limits, the scan is restarted. If out of limits, fast scan is reentered before the calibration point.

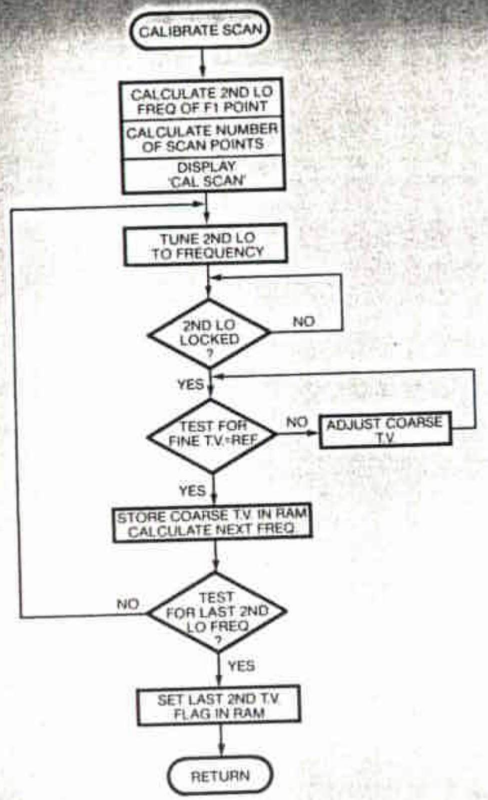

Figure 9. Flow chart of fast-scan calibration.

When end-of-scan is not detected, the LOG video A/D is read. The LOG reading is tested against the COR LEVEL to decide if a signal is present. On signal acquisition, a routine called "SIGNAL QUE" decides if the signal is real, and if so, loads a buffer along with telling the outside world about it. If it decides that there is no signal, control is returned to FAST SCAN. Here, a test is made for end-of-voltage table; if, at the end, the 1st LO is incremented or decremented according to step size, being positive or negative indicates scan up or scan down. The loop is reentered at the send voltage code point when the end of the 2nd LO range is not detected. This has been a basic description of how the FAST SCAN functions.

Built-in-test and Diagnostics

Built-in-test (BITE) can no longer be considered an optional enhancement to a digitally controlled receiver. The mission of signal collection sites is to collect, record and classify as many signals as possible. A main computer can work many signals simultaneously, and may be only limited to the number of receivers under remote control. New compact receivers make possible hundreds of receivers per rack. BITE, under remote control, is no longer a luxury but a mandatory requirement of the collection system.

Hardware has turned into software and is, of course, more reliable. However, receiver test and repair have, unfortunately, turned into a maze of strange terms to the average technician.

As equipment grows in complexity and software dependence, the requirement for a useful, dependable diagnostic system also grows. Fortunately, the ability to provide such a system also grows as software takes control of functions that were predominately done in closed hardware loops. The software must go beyond just testing the receiver to help the maintenance personnel isolate a problem. The internal relationship of the software to the proper function of modes such as AGC, AFC, and BFO could make fault isolation a task that could be only done by the original design team. Such a situation is entirely unacceptable. The solution is to include diagnostics in the standard receiver software.

The diagnostics should include both digital and analog parts of the system. Many of software diagnostics can be done with little or no additional hardware requirements. Examples include RAM, ROM and timer tests in the digital section. Many receiver functions such as AM detector, LOG detector, AM PEAK detector, AM AC detector, FM discriminator, IF bandwidths, LO lock ups, and attenuators can be all tested, and fault isolated by tuning to or near 0 MHz.

Other areas such as power supplies, audio outputs, analog-to-digital converter and references may be checked with very minor hardware additions. The usefulness and value of the software diagnostics are only limited by the designer's ability to transfer his expertise into a working software package.

Overview of Receiver Diagnostics

The receiver diagnostics can be grouped in two basic classes. Those required to verify the most basic functions and those oriented around finding more subtle faults which may not make the receiver totally inoperative. Those diagnostics required to verify basic functions should be run at regular intervals, such as power-up, if they can be done in a timely manner. Those looking for not-so-obvious faults can be run at the operators discretion, when execution time is not a factor.

The tests run at power-up may be separated into two areas, digital (shown in Figure 10) and analog (shown in Figure 11). Since all testing is under control of the digital section, it makes good sense to verify this section first. This helps certify that faults found later in the diagnostics are real and not ones created by bad inputs from the digital section. All the faults found in this area are assumed fatal. This means that upon finding a fault, the display indicates a fatal fault and never passes control to the actual system software. All the diagnostics reside in EPROM, so, what is a more likely candidate to test first? A checksum routine provides a good verification of proper EPROM operation. RAM operation is a requirement to provide proper digital section functions; therefore, it is tested next using a non-destructive memory test to avoid destroying stored setups. The A/D converter is required for receiver functions to operate; therefore, it and ±15 voltages are tested. By summing supply voltages at an A/D input, the voltages and A/D may be verified. Interrupt timers, which are required for proper software operation, can be timed before passing them to the operating system. The BFO counter interrupt may also be tested. All of the digital section tests can be executed in the time

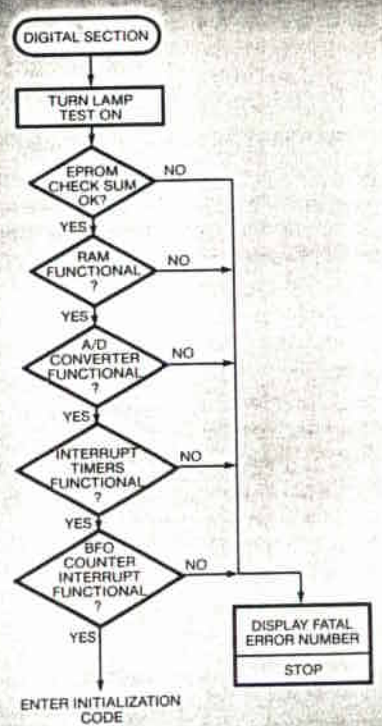

Figure 10. Flow chart of power-up digital diagnostics.

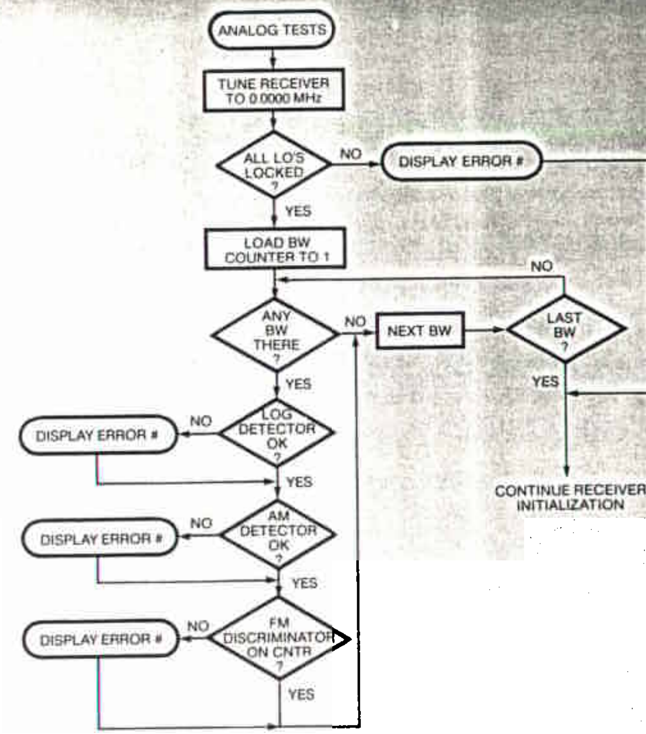

Figure 11. Flow chart of power-up analog diagnostics.

allotted to allow the analog circuits to stabilize. A lamp test is a good consideration while these tests are taking place. Fault isolation in the digital section is done with SIGNATURE ANALYSIS PROGRAMS stored in the operating system EPROM, which the user can start by a special sequence. These programs will exercise all the digital section outputs, in a documented sequence. All these functions are implemented with almost no increase in hardware costs.

The analog tests run at power-up are meant to provide a minimum operator verification of a functional receiver. Faults detected are not completely fatal, so only an error number is displayed during power-up. Then, the operator is given normal control, if possible. The test sequence starts by tuning the receiver to 0 MHz and watching the lock indicator. The LO lock indicators are continuously monitored in the operating system software so the operator is immediately aware of a fault. Next is the verification of the log detector, AM detector, and FM discriminator, in each bandwidth. These tests provide a minimum verification of a functional receiver at only a penalty of about one second, at power-up time.

The fault isolation tests are designed to concentrate on the analog receiver functions. These include LO tests at all frequencies of each LO. With the receiver at 0 MHz, a level measurement of the LO is made with the LOG detector. Then, each of the voltage control attenuators are moved and the change is limit-checked on the LOG detector. By looking at the results, a fault may be isolated to an attenuator or the LOG detector. After the attenuators are verified, the AM detector is checked for consistency with a curve stored in PROM. Differences from this curve could cause improper function of the AGC loop.

Each bandwidth is measured and compared with the identified value. FM discriminator center and slope are verified in each bandwidth. The FM AC and AM AC detectors are verified by stepping between zero and the bandwidth edge. This creates a signal with both AM and FM modulation. By narrowing the step to inside the bandwidth edges, only FM is present. Now the video switch is set in FM, and audio outputs are checked. Again with AM selected, the audio is tested for signal absence. FM quieting can also be tested to verify receiver performance. This is only a start to what can be tested with software.

Conclusion

The hardware circuitry of a digitally controlled receiver can be greatly reduced by software design. New functions can be implemented that improve the receiver's performance that are not possible in hardware. Synthesizers may be built and tested to the lowest possible phase noise with no adjustments. Software driven built-in-test and diagnostics are no longer optional considerations with remotely controlled receiving systems. The software complexity of design now requires more engineering development time, but substantially reduces the recurring costs.

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